Attorney Docket No.: 0180139

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Kluth, et al.**

Serial No.: 10/655,179

Filed: September 4, 2003

For: **Memory Cell Structure Having Nitride Layer with Reduced Charge Loss and Method for Fabricating Same**

Art Unit: 2818

Examiner: Tran, Long K.

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-6 and 14-19. The Final Rejection issued on April 25, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on July 21, 2005.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-6 and 14-19 are pending, and claims 7-13 and 20 were canceled in previous amendments. Claims 1-6 and 14-19 have been finally rejected in a Final Rejection dated April 25, 2005. This Appeal is directed to the rejection of claims 1-6 and 14-19, which appear in the attached "Appendix of Claims on Appeal."

STATUS OF AMENDMENTS

No claim amendments have been submitted in response to or subsequent to the Final Rejection dated April 25, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 is directed to a memory cell structure (e.g., structure 100 in Figure 1) comprising a semiconductor substrate (e.g., substrate 110 in Figure 1), a first silicon oxide layer (e.g., layer 115 in Figure 1) over the substrate, a charge storing layer

(e.g., layer 120 in Figure 1) over the first silicon oxide layer, where the charge storing layer has a reduced hydrogen content that in turn reduces charge loss in the charge storing layer. Independent claim 1 further claims a second silicon oxide layer (e.g., layer 125 in Figure 1) over the charge storing layer, and a gate layer (e.g., layer 130 in Figure 1) over the second silicon oxide layer. *See, e.g., page 8 of the present application, lines 1-22.*

It is noted that the detailed description of the present invention further defines and explains the phrase "silicon nitride having reduced hydrogen content" as used in claim 1 to refer to charge storing layer 120. For example, the present application states: "Nitride layer 120 comprises a unique silicon nitride (Si_3N_4) layer having significantly reduced hydrogen content. For example, hydrogen content in nitride layer 120 may be in the range of about 0 to 0.5 atomic percent, which is a significant hydrogen content reduction over conventional nitride layers having a hydrogen content of about 1 to 2 atomic percent." *See, e.g., page 8 of the present application, lines 13-18.* Moreover, exemplary methods for fabricating the "silicon nitride having reduced hydrogen content" are disclosed and described in relation to flowchart 300 in Figure 3, and flowchart 400 in Figure 4. *See, e.g., page 10 of the present application, line 21 through page 14, line 17.*

As a result of the invention claimed by claim 1, charge loss in memory cells is significantly reduced, thus resulting in longer retention of memorized data.

B. Claim 14

Independent claim 14 is directed to substantially the same subject matter as independent claim 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-3, 6, 14-16, and 19 under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,740,605 to Shiraiwa et al. (hereinafter "Shiraiwa").

B. Claims 4-5 and 17-18 stand rejected under 35 U.S.C. §103 as being unpatentable over Shiraiwa.

ARGUMENT

A. Rejection of claims 1-3, 6, 14-16, and 19 under 35 U.S.C. §102(b) as being anticipated by Shiraiwa

The Examiner has rejected claims 1-3, 6, 14-16, and 19 under 35 USC § 102(e) as being anticipated by Shiraiwa. For the reasons discussed below, Applicant submits that the present invention, as defined by independent claims 1 and 14, is patentably distinguishable over Shiraiwa.

Shiraiwa is directed to a process for fabricating a semiconductor device that is less susceptible to performance degradation caused by hydrogen contamination. Shiraiwa discloses steps for removing unwanted hydrogen bonds after the nitride layer is formed by exposing the hydrogen bonds to ultraviolet radiation sufficient to break the bonds, and then annealing in an atmosphere using a gas, such as oxygen (O_2), ozone (O_3), or a source

of nitrogen such as NO, N_2O, or N_2, capable of forming bonds that replace the hydrogen bonds. *See Figure 12 of Shiraiwa and related description on column 11. See also column 10, line 50 through column 11, line 20.*

However, as the Examiner has acknowledged, Shiraiwa does not disclose a motivation to reduce charge loss by reducing hydrogen content, but simply a desire to reduce hydrogen content to reduce contamination and a "hypothesis" that hydrogen migration into bottom or top oxide dielectric layers can cause undesirable effects by changing the "barrier height" in those layers. As the Examiner has further acknowledged on page 8, paragraph 11 of the Final Office Action, Shiraiwa is completely silent as to how hydrogen content in the nitride layer itself results in threshold voltage shifting, and a desire to reduce hydrogen content in the nitride to reduce charge loss in the nitride layer itself is not taught by Shiraiwa. *See, for example, column 2, lines 29-49 of Shiraiwa.*

In contrast, referring to Figure 1 of the present application, due to the reduced hydrogen content in nitride layer 120, the amount of hydrogen radicals than can be freed in nitride layer 120 during subsequent programming operations is greatly reduced. Consequently, the charge loss in nitride layer 120 is significantly reduced. As a benefit, the reduction of charge loss in nitride layer 120 significantly reduces the threshold voltage shift in resulting memory cell structure 100. *See, for example, the present application page 9, lines 1-6.* Moreover, the present invention requires use of highly reactive nitrogen radicals in a unique CVD process to minimize number of hydrogen radicals. As stated in the present application at step 320 in flowchart 300, a unique CVD process is

used to form a nitride layer having reduced charge loss over the first oxide layer. In an exemplary embodiment, a precursor comprising silane and a highly reactive form of nitrogen is used in a CVD process at a temperature of about 400 to 650° C. For example, microwave energy, or other similar processing, may be use to break up nitrogen (N_2) into a highly reactive form of nitrogen, i.e. to form "nitrogen radicals." With the unique CVD process described above, a nitride layer having significantly reduced hydrogen content is achieved. As discussed above, the reduced hydrogen content in the nitride layer results in a nitride layer having reduced charge loss. With reference to Figure 2, nitride layer 220 is formed over first oxide layer 215 during step 320. *See, for example, the present application page 11, lines 13-22 and Figures 2 and 3.*

B. <u>Rejection of claims 4-5 and 17-18 under 35 U.S.C. §103 as being unpatentable over Shiraiwa</u>

The Examiner has rejected dependent claims 4-5 and 17-18 under 35 U.S.C. §103 as being unpatentable over Shiraiwa. For the reasons discussed below, Applicant submits that the present invention, as defined by dependent claims 4-5 and 17-18, is patentably distinguishable over Shiraiwa.

As disclosed in the present application and claimed in claims 4-5 and 17-18, the unique technique of the present invention results in a charge storing layer having "a hydrogen content less than 1.0 atomic percent," or a charge storing layer having "a hydrogen content between 0 and 0.5 atomic percent."

Although the Examiner has acknowledged the lack of any teaching or motivation

in Shiraiwa regarding reducing charge loss through a deliberate reduction of hydrogen content in the nitride layer, the Examiner has stated that the resulting products "seem to be identical" and further the limitation of forming the charge storing layer from nitrogen radicals does not result in a patentable product. However, the resulting product according to the present invention is patentably distinguishable over Shiraiwa's product and, in particular, claims 4-5 and 17-18 are further distinguishable over Shiraiwa. As stated in Shiraiwa:

> "The high-K dielectric material may be formed by reacting a suitable metal-containing gas, e.g., hafnium tetra-t-butoxide with a suitable oxygen-containing gas, e.g., oxygen (O_2) or nitrous oxide (N_2O). In one embodiment, the storage material may be deposited by chemical vapor deposition (CVD) methods. The CVD method may be any appropriate CVD method-known in the art for deposition of a high-K material. For example, the CVD method may be ALD (ALCVD), PECVD, MOCVD or MLD, in addition to the above-mentioned RTCVD. In one embodiment, PECVD is used to deposit the charge storage layer 30. The charge storage layer may also be deposited by other suitable methods. It will be understood that the conventional methods detailed above impart significant hydrogen content into the charge storage layer 30 and interface 36 in the form of dielectric-hydrogen bonds. <u>The hydrogen content may range from greater than 3 atomic percent up to as much as 30 atomic percent, and in some cases may be greater than 8 atomic percent, and in other cases may range, from about 10 atomic percent to as much as 30 atomic percent</u>. For example, in conventional depositions of silicon nitride charge storage layers 30, a significant proportion of the hydrogen present at the interface 36 is present in the form of Si--H bonds, and the hydrogen content may be as high as 30 atomic percent. In one embodiment, in the next step of the present invention, shown schematically in FIG. 11 as step 1108, the process comprises irradiating the interface 36 with ultraviolet radiation. In one embodiment, the ultraviolet radiation is applied at an energy in the range of about 3 eV to about 8 eV. In one embodiment, the UV is applied at an energy of at least 3.3 eV. In one embodiment, the UV radiation is applied at an energy of at least 3.9 eV. In one embodiment, the UV radiation is applied at a dose and energy sufficient to break at least one of dielectric-hydrogen bonds, e.g., silicon-hydrogen and/or nitrogen-hydrogen

> bonds. In one embodiment, the UV radiation comprises a wavelength ranging from about 160 nm to about 400 nm." *Column 10, line 50 through column 11, line 20 of Shiraiwa (emphasis added).*

As stated in Shiraiwa, the "hydrogen content may range from greater than 3 atomic percent up to as much as 30 atomic percent, and in some cases may be greater than 8 atomic percent, and in other cases may range, from about 10 atomic percent to as much as 30 atomic percent." *Column 10, line 65 through column 11, line 3 of Shiraiwa.* One reason for this high hydrogen content is that Shiraiwa does not utilize the nitrogen radical process of the present invention. Regardless of the reason, Shiraiwa acknowledges that such hydrogen content of up to 30 atomic percent is high, but does not disclose any specific reduced level of hydrogen content that Shiraiwa does achieve. More particularly, Shiraiwa does not disclose that the hydrogen content is reduced to less than 1.0 atomic percent, or is reduced to between 0.0 and 0.5 atomic percent. Thus, Applicant submits that not only Shiraiwa is silent as to a nitride charge storage layer formed by nitrogen radicals, but also the Shiraiwa's nitride layer is patentability distinguishable since it does not achieve a hydrogen content less than 1.0 atomic percent, or between 0.0 and 0.5 atomic percent, as disclosed and claimed by dependent claims 4-5 and 17-18 in the present application.

CONCLUSION

Based on the foregoing reasons, independent claims 1 and 14, and claims depending therefrom and, in particular, dependent claims 4-5 and 17-18, claim inventions that are patentably distinguishable over Shiraiwa. As such, and for all the foregoing

reasons, an early allowance of claims 1-6 and 14-19 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
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Date: 9/22/05

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Christina Carter 9/22/05
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A memory cell structure comprising:

a semiconductor substrate;

a first silicon oxide layer situated over said semiconductor substrate;

a charge storing layer formed from nitrogen radicals and situated over said first silicon oxide layer, said charge storing layer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer;

a second silicon oxide layer situated over said charge storing layer;

a gate layer situated over said second silicon oxide layer.

Claim 2: The memory cell structure of claim 1, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 3: The memory cell structure of claim 2, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

Claim 4: The memory cell structure of claim 1, wherein said charge storing layer has a hydrogen content less than 1.0 atomic percent.

Claim 5: The memory cell structure of claim 1, wherein said charge storing layer has a hydrogen content between 0 and 0.5 atomic percent.

Claim 6: The memory cell structure of claim 1, wherein said charge storing layer is capable of storing two bits.

Claim 14: A memory cell structure comprising:

a semiconductor substrate, a first silicon oxide layer situated over said semiconductor substrate, a charge storing layer situated over said first silicon oxide layer, a second silicon oxide layer situated over said charge storing layer, a gate layer situated over said second silicon oxide layer, said memory cell structure characterized by:

said charge storing layer formed from nitrogen radicals and comprising silicon nitride having reduced hydrogen content;

said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 15: The memory cell structure of claim 14, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 16: The memory cell structure of claim 14, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

Claim 17: The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content less than 1.0 atomic percent.

Claim 18: The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content between 0 to 0.5 atomic percent.

Claim 19: The memory cell structure of claim 14, wherein said charge storing layer is capable of storing two bits.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)